



## PART B - FEE(S) TRANSMITTAL

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XILINX, INC  
ATTN: LEGAL DEPARTMENT  
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SAN JOSE, CA 95124

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Pat Tompkins (Depositor's name)  
Pat Tompkins (Signature)  
October 20, 2006 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10796,475	03/09/2004	Stephen M. Trimberger	X-812-IP US	2300

TITLE OF INVENTION: FPGA CONFIGURATION MEMORY WITH BUILT-IN ERROR CORRECTION MECHANISM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$0	\$0	\$1400	12/27/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
SIDDIQUI, SAQIB JAVAID	2138	714-746000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
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2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,  
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1. LeRoy D. Maunu

2.

3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

XILINX, INC.

San Jose, California 95124

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee  
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☒ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Date October 20, 2006

Typed or printed name

Keith A. Chanroo

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This collection of information is required by 37 CFR 1.511. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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P. O. Box 1450

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22313-1450

Inventor(s): Stephen M. Trimberger et al.

Assignee: XILINX, INC.

Serial No.: 10/796,475

conf.no. 2300

Filed: March 9, 2004

Title: FPGA Configuration Memory with Built-In Error Correction Mechanism

Docket No.: X-812-1P US

Enclosed: Return Receipt Postcard

Fee Transmittal - Part B

Date: October 20, 2006

VIA FACSIMILE 571-273-2885

Atty/Sec: KAC/pat

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